claim 122 limitations. Claim 122 does not say that the recited active element is "on or in" the insulating layer. Claim 122 states that **the insulating layer is processed to produce an active device.**

As but one example, it is well known to pattern etch an insulator provided over a semiconductor substrate and dope the substrate to form source/drain regions of a transistor and fabricate a conductor structure over the insulator to form a transistor gate. Silicon can also be provided over or within an insulator to provide a silicon-on-insulator (SOI) substrate which can support active devices. There is also ample support in the specification to teach one skilled in the art how to process an insulating layer which is provided over a semiconductor substrate to produce at least one active device. For example, the specification states "**[a]lternatively**, the interposer substrate 100 **may also** have active devices built on or into the insulating layers 104 on one or both sides of the substrate 100." Specification at page 19, lines 11-13 (emphasis added). For further support, the Examiner is directed to US Patents 5,691,230, 5,767,563, 5,786,250, and 5,858,845, all of which were available at the time the present invention was filed, and all of which disclose SOI techniques in which active devices are built on an insulating layer. Copies of these patents are being submitted with this Amendment.

In response to the Examiner's question "how can an active circuit be formed in an insulating layer?" (page 2, section 1), the Examiner is again reminded that this is not what claim 122 recites and, in any event, the manner in which this can occur has been explained, for example, by removing at least portions of the insulation layer during transistor formation. In response to the Examiner's question "is this the same insulating layer that carries the passive circuit element?" (page 2, section 1), the claim 122 language is clear. It states that the insulating layer having the passive device is "processed" to produce an active device. Finally, in response to the Examiner's other question, a passive circuit element is not the same as an active circuit element.

Claim 88 stands rejected under 35 U.S.C. §103 as unpatentable over Stone in view of Yamazaki (page 3, paragraph 1). Claim 88, as amended, now recites a process for

forming an interposer element for use as a chip carrier comprising the steps of:

> providing an insulating layer on at least one surface of a silicon substrate; and
>
> processing said insulating layer to produce at least one passive circuit element on or within said insulating layer, said at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer, said portion of said insulating layer having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate,
>
> **bonding at least one integrated circuit chip to said interposer element** such that said at least one integrated circuit chip is electrically connected to said at least one passive circuit element; and
>
> **forming a metallization pattern** on or within said insulating layer, said metallization pattern being connected with said at least one passive circuit element. (emphasis added)

As previously noted in the Amendment filed October 26, 2001 the amended claim 88 recites bonding at least one integrated circuit chip to said interposer element such that said at least one integrated circuit chip is electrically connected to said at least one passive circuit element, as emphasized above. The Office Action again states that this feature can be found within Stone's Figure 2 (page 3, paragraph 2). Stone's Fig. 2 shows an interposer 100 with electronic devices 31, 33 joined on either side (col. 8, lines 31-36). Separately, Stone contemplates forming passive electronic components within the interposer layer 100. However, nowhere within the Stone reference, and certainly not within Figure 2, does Stone disclose an integrated circuit chip being electrically connected to a passive circuit element formed within an interposer layer, as claimed. For at least the above reasons, the rejection of claim 88 and all claims dependent therefrom should now be withdrawn.

Additionally, the subject matter of claim 96 has been incorporated into independent claim 88, also as emphasized above, and claim 96 has been cancelled. The claimed step of forming metallization patterns is advantageous because doing so results in compact architectures and improved performance due to a reduction in the parasitic effects

attributed to wire bonds (page 16, lines 1-2). In rejecting claim 96, the Office Action asserted that Stone's conductive layer 21 suggests the claimed metallization layer. This assertion is respectfully traversed in that Stone's conductive layer 21 is not anywhere described as have metallization patterns located thereupon, or describe use of metallization for connecting a passive device formed within an insulating layer within a chip. For at least the above reasons, the rejection of claim 88 and all claims dependent thereupon should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

88 (amended) A process for forming an interposer element for use as a chip carrier comprising the steps of:

providing an insulating layer on at least one surface of a silicon substrate; and

processing said insulating layer to produce at least one passive circuit element on or within said insulating layer, said at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer, said portion of said insulating layer having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate,

bonding at least one integrated circuit chip to said interposer element such that said at least one integrated circuit chip is electrically connected to said at least one passive circuit element; and

forming a metallization pattern on or within said insulating layer, said metallization pattern being connected with said at least one passive circuit element.

96. (cancel without disclaimer or prejudice)